DMACONT PAGE 1

1 ;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

2 ;

3 ; Author : ADI - apps www.analog.com/MicroConverter

4 ;

5 ; Date : October 2003

6 ;

7 ; File : DMAcont.asm

8 ;

9 ; Description : performs continuous mode DMA conversions on a

10 ; single ADC channel at 138KSPS (assuming an

11 ; 11.0592MHz Mclk).

12 ; Debugger or emulator must be used to view results.

13 ;

14 ;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

15

16 $MOD841 ; use 8052&ADuC841 predefined symbols

17

0040 18 DMACOUNT EQU 64 ; number of AD readings to take

0010 19 DMAINIT EQU 10h ; top nibble of DMAINIT = ADC channel

20

21 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

22 ; DEFINE VARIABLES IN INTERNAL RAM

---- 23 DSEG

0060 24 ORG 0060h

0060 25 DMASTOPH: DS 1 ; DMA stop address hi byte

0061 26 DMASTOPL: DS 1 ; DMA stop address lo byte

27

28 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

29 ; DEFINE SEGMENT OF EXTERNAL RAM

---- 30 XSEG

0000 31 ORG 000000h

0000 32 DMASTART: DS DMACOUNT\*2 ; location for DMA results

0080 33 DMASTOP: DS 4 ; location for DMA stop sequence

34

35 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

36 ; BEGINNING OF CODE

---- 37 CSEG

0000 38 ORG 0000h

0000 02004B 39 JMP MAIN ; jump to main program

40

41 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

42 ; INTERRUPT VECTOR SPACE

0033 43 ORG 0033h ; (ADC ISR)

0033 C2DD 44 CLR CCONV ; stop conversions

0035 C3 45 CLR C ; clear C to indicate DMA done

0036 32 46 RETI

47

48 ;====================================================================

49 ; MAIN PROGRAM

004B 50 ORG 004Bh

004B 51 MAIN:

52

53 ; PRECONFIGURE external RAM for DMA capture on a single channel...

004B 75EF00 54 MOV ADCCON1,#00h ; set MD1, MD0 TO 0

55

004E 900080 56 MOV DPTR,#DMASTOP ; store DMASTOP 16bit value..

0051 858261 57 MOV DMASTOPL,DPL ; ..as a high byte & low byte

0054 858360 58 MOV DMASTOPH,DPH ; (for use in GETSTOPFLAG subr)

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0057 900000 59 MOV DPTR,#DMASTART ; set DPTR to DMASTART address

005A 7410 60 SETUP: MOV A,#DMAINIT ; set up x-mem with init value

005C F0 61 MOVX @DPTR,A

005D A3 62 INC DPTR

005E E4 63 CLR A ; clear second byte

005F F0 64 MOVX @DPTR,A

0060 A3 65 INC DPTR

0061 12008B 66 CALL GETSTOPFLAG ; C cleared if DPTR>=DMAEND

0064 40F4 67 JC SETUP

68

0066 7410 69 MOV A,#DMAINIT ; "dummy" DMA location..

0068 F0 70 MOVX @DPTR,A ; ..to preceed stop command

0069 A3 71 INC DPTR

006A E4 72 CLR A

006B F0 73 MOVX @DPTR,A

006C A3 74 INC DPTR

75

006D 74F0 76 MOV A,#0F0h ; DMA stop command

006F F0 77 MOVX @DPTR,A

78

79 ; CONFIGURE ADC for DMA conversion...

80

0070 75D200 81 MOV DMAL,#0 ; start address for DMA operation

0073 75D300 82 MOV DMAH,#0 ; (must write DMA registers in this

0076 75D400 83 MOV DMAP,#0 ; order: DMAL, DMAH, DMAP)

84

0079 75D840 85 MOV ADCCON2,#040h ; enable DMA mode

007C 75EF9C 86 MOV ADCCON1,#09Ch ; 7.2us conv+acq time

87

007F D2AF 88 SETB EA ; enable interrupts

0081 D2AE 89 SETB EADC ; enable ADC interrupt

90

91 ; LAUNCH DMA conversion... when complete, ADC interrupt will clear C

92

0083 D2DD 93 SETB CCONV ; start continuous ADC conversions

0085 D3 94 SETB C

0086 40FE 95 JC $ ; wait for DMA to finish

96

0088 00 97 NOP ;.................................... SET BREAKPOINT HERE

98

99 ; REPEAT entire program...

100

0089 80C0 101 JMP MAIN

102

103 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

104 ; SUBROUTINE

105

008B 106 GETSTOPFLAG: ; clears C if DPTR>=DMASTOP

008B D3 107 SETB C

008C E583 108 MOV A,DPH

008E B56005 109 CJNE A,DMASTOPH,RET1 ; C cleared if DPH>=DMASTOPH

0091 E582 110 MOV A,DPL

0093 B56100 111 CJNE A,DMASTOPL,RET1 ; C cleared if DPL>=DMASTOPL

0096 22 112 RET1: RET

113

114 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

115

116 END

VERSION 1.2h ASSEMBLY COMPLETE, 0 ERRORS FOUND

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ADCCON1. . . . . . . . . . . . . D ADDR 00EFH PREDEFINED

ADCCON2. . . . . . . . . . . . . D ADDR 00D8H PREDEFINED

CCONV. . . . . . . . . . . . . . B ADDR 00DDH PREDEFINED

DMACOUNT . . . . . . . . . . . . NUMB 0040H

DMAH . . . . . . . . . . . . . . D ADDR 00D3H PREDEFINED

DMAINIT. . . . . . . . . . . . . NUMB 0010H

DMAL . . . . . . . . . . . . . . D ADDR 00D2H PREDEFINED

DMAP . . . . . . . . . . . . . . D ADDR 00D4H PREDEFINED

DMASTART . . . . . . . . . . . . X ADDR 0000H

DMASTOP. . . . . . . . . . . . . X ADDR 0080H

DMASTOPH . . . . . . . . . . . . D ADDR 0060H

DMASTOPL . . . . . . . . . . . . D ADDR 0061H

DPH. . . . . . . . . . . . . . . D ADDR 0083H PREDEFINED

DPL. . . . . . . . . . . . . . . D ADDR 0082H PREDEFINED

EA . . . . . . . . . . . . . . . B ADDR 00AFH PREDEFINED

EADC . . . . . . . . . . . . . . B ADDR 00AEH PREDEFINED

GETSTOPFLAG. . . . . . . . . . . C ADDR 008BH

MAIN . . . . . . . . . . . . . . C ADDR 004BH

RET1 . . . . . . . . . . . . . . C ADDR 0096H

SETUP. . . . . . . . . . . . . . C ADDR 005AH